Description of the electronic logic in GRAAL (see scheme electr4.ps)

1 From individual pulses to charge and sequence trigger

The light of the Cherenkov showers reflected by the heliostats is collected in 4 Winston cones which have each 1 PMT attached at its focus.
Every pulse arriving to any of the PMTs is amplified with 2 amplifiers ORTEC with a band width (BW) of $\approx$ 400MHz. The pulse is then directed both to an electronic system (which makes the coincidences and decides whether the event was real or only noise) and to the scope (which registers the event in case it passes the trigger).
The trigger consists of 2 components, **sequence** and **charge** trigger. The first one is performed in cones 1 and 2 and the second one in all 4 cones.
After entering the *Linear Fan I/O 428F* the pulses are directed to a discriminator *module 623 LRS* and to an integrator *Fast Filter Amplifier EG+G 579*. I'll denote the pulses going to the integrator as **branch 1** and the ones going to the discriminator as **branch 2**. There is a third output of the *Linear Fan I/O 428F* which goes to the *ADC 2249W* to have an independent measurement of the charge of the traces.
In cones 1 and 2 the charge of the pulses is integrated during as time of 100ns and the resultant pulse is discriminated in *module 621 CL* with a threshold of 35mV, whereas for cones 3 and 4, the integration is made during a time of 200ns and the resultant pulse is discriminated in *module 621 BBL* with the same threshold as for cones 1 and 2. This difference is due to the fact that cones 3 and 4 receive the light from heliostats which are further away than 1 and 2, and consequently the total light intensity is lower. All these 4 integrated and already discriminated pulses are introduced in a *majority coincidence unit* (consistent at the moment in a module *Linear Fan I/O 428F* followed by a discriminator *624*, an attenuator must be introduced between both modules for operating properties of the discriminator). This coincidence unit decides whether the pulses have passed or not the charge trigger. The condition for a positive trigger is that 3 of the 4 integrated pulses are over the threshold of the discriminators.
The pulses of the **branch 2** of the scheme suffer different processes depending on the cones. For cones 1 and 2 the pulses go through a logic which determines the sequence trigger, whereas for cones 3 and 4, the pulses are simply sent to counters after being discriminated with a threshold of 30mV in module *623*.
For the sequence trigger 3 pulses higher than a threshold of 30mV in a total time of 30 ns are required. This is implemented as follows: the pulses arrive to the module *Logic Fan*

I/O 429 with a width of 10ns. The first pulse arriving to the module is delayed by a 8ns cable and introduced in an AND gate *coincidence unit 622*. If a second pulse arrives in the 8ns following the arrival of the first pulse, they will be in coincidende in the AND gate, and the output of such gate will be a pulse which is again delayed 8ns and introduced in a second AND gate. If a third enters an AND gate together with the result of the first AND gate, the sequence trigger is fired. The pulse indicating a sequence trigger (SEQ 1) enters a module *Linear Fan I/O 428F* (AND3 gate) together with the result of the charge trigger for the respective cone. If either the sequence or the charge trigger have been fired, an output pulse is directed to an AND gate *coincidence unit 465*. If in both cones 1 and 2 the output signal of AND3 is 1 logic the sequence trigger will be fired.

2 From charge and sequence trigger to total trigger

At this stage there are 2 logic pulses, corresponding to the result of the charge and sequence trigger. To have a total trigger positive (1) signal, one of both pulses has to be positive. In the second part of the scheme, which begins now (having already a pulse of the charge trigger and another of the sequence trigger), the vetos (blue cables) for busy PC are set and the events are registered.

Both sequence and charge trigger pulses enter 2 modules, a *Logic Fan I/O 429* and an AND gate in module *364 ALP*. The pulse of the charge trigger passes through a *Logic Unit 365AL* which has 2 vetos as input apart from the pulse. The first veto is set by the charge pulse itself, the pulse is directed to a pulse generator (1.1) , which sets a dead time of 0.1ms for reading another pulse in the *module 364AL*. The second veto comes from *Camac module C219* and is set by the computer, i.e., the dead time of the computer determines whether such computer is ready to accept a new pulse or not. If the coputer is not ready, any pulse arriving to *Logic Unit 365AL* will be lost.

In AND*2 Gate *module 364ALP* something similar occurs. 2 vetos are also introduced as input through a *module 429, Logic Fan I/O* (one blue cable). The first veto is introduced as in previous case through a *pulse generator (2.1)*, which sets a dead time of 10 ms once that either the charge or the sequence pulse have arrived to the *module 364ALP*. The second veto is again set by the PC and comes from *Camac module C219*. If none of the 2 vetos is positive, the event can be registered, i.e., a master pulse is the 1 logic output of the module, which tells the computer that the event can be recorded. There is one last input introduced to AND*2 Gate and *module 429, Logic Fan I/O* which is only used for tests. In the normal run conditions, the module *dual gate pulse generator (2.2)* which doesn't have any effect, since no input is introduced to it. However, when making tests, such module

is set to 'oscillator mode' and a signal with a frequency of 10MHz is sent to the modules indicated before.
The calibrations can be performed by a Philips module or by 4 LEDs attached to the cones on their glass surface.
The Philips module (in the CAMAC crate) sends 4 signals exactly after the PMT and before the first amplifier whenever it receives the order from computer. The other signal to be sent from Philips is a signal to the MASTER (in module *Logic Fan I/O 429*). The master signal is sent on purpose to have always the same trigger time. Since the amplitude of the pulses change for different calibrations, the trigger time also changes, but we want to have always the same time. This signal to the MASTER goes through a module *TTL-NIM-TTL Adapter*.
For the calibration with the 4 LEDs, a signal is sent from computer (via *Camac module C219*) and through a module *Logic Fan I/O 429* 4 signals are sent to the LEDs. As in Philips module, a signal has to be sent also to the MASTER, it is made by the *Camac module C219* (through cable LP CAL). Thus, to the *module 429 Logic Fan I/O* 3 signals arrive, the master for real events and the master for the 2 calibrations. Any of these 3 pulses goes twice into the *ADC 2249W* (one for the gate of the module and another one for the signal) and to the *scope*. The signal which goes to the gate of the *ADC 2249W* passes through a *dual gate pulse generator (2.1)* which sets a dead time of 500ns to allow the ADC to register the whole traces of S1, S2, S3 and S4. The input to the scope is made via a *429A module Logic Fan I/O* with second input the computer trigger. Whenever the *Camac module C219* sends a positive pulse to the *429A module* and the master pulse is positive, the event is sent to the scope.